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February 8, 1963

APPLICATION OF SEMICONDUCTOR DEVICES TO HIGH POWER DUPLEXERS

Prepared by:

Joseph White

MICROWAVE ASSOCIATES, INC.
BURLINGTON, MASSACHUSETTS

Third Quarterly Progress Report
1 August 1962 to 31 October 1962
Contract No. AF30(602)-2656

Prepared for:

Rome Air Development Center
Research and Technology Division
Air Force Systems Command
United States Air Force
Griffiss Air Force Base, New York

MICROWAVE ASSOCIATES, INC.

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February 7, 1963

Third Quarterly Progress Report

1 August 1962 to 31 October 1962

APPLICATION OF SEMICONDUCTOR DEVICES TO HIGH POWER DUPLEXERS

Prepared by:

Joseph White

Approved by:

M. E. Hines

MICROWAVE ASSOCIATES, INC.
BURLINGTON, MASSACHUSETTS

Contract No. AF30(602)-2656

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Task No. 450602

Prepared for

Rome Air Development Center

Research and Technology Division

Air Force Systems Command

United States Air Force

Griffiss Air Force Base

New York

ABSTRACT

The purpose of this program is to recommend semiconductor duplexing techniques which show promise for extending the power handling capability of semiconductors when used as duplexers. The program for this quarter had the following aspects:

(1) The building of packaged PIN diodes to meet the design criteria set forth in the last quarter.

(2) The design and building of an integrated semiconductor duplexer structure to maximize the heat dissipation and power handling capabilities of the structure.

(3) Design of the semiconductor junction to minimize the thermal dissipation, the turn-on time, and the series resistances.

The progress made in this quarter on these aspects will be described in the following report.

TABLE OF CONTENTS

I INTRODUCTION

The semiconductor element offers great promise as a microwave duplexing element. Its nonlinear characteristics together with a fast response make it useable at microwave frequencies as a limiter or duplexer. The feasibility of a 1 Mw peak power, 1000 watt average power semiconductor duplexer was discussed in the Rome Air Development Center PR #152172. Basically, this program requires the development of a very high power primary limiter stage to reduce the incident power to a level which can be handled by already developed semiconductor limiter or duplexer circuits. This approach appears feasible if the semiconductor structure can be integrated directly into the microwave transmission line, thus greatly enhancing the heat dissipating characteristics of the diode. Our approach will be to integrate a PIN junction which because of its inherent high voltage characteristics and its low capacitance per unit area will be able to handle large peak and average microwave power. However, a PIN junction requires a finite time for the carriers to be injected into the I-region. During this time the limiter will pass a spike. This spike leakage then can be eliminated by a succeeding duplexer stage which employs varactor diodes which will not handle high power, but by reacting more rapidly will eliminate the spike.

The present approach is then to build an integrated PIN limiter that has the maximum power dissipation obtainable and rapid response to keep the spike leakage to be handled by the varactor limiter to a minimum. Our approach to building this limiter has centered on the PIN

semiconductor junction. We are building a reliable passivated diode with a minimum series resistance and the maximum heat dissipation which can be integrated directly into the duplexer. The work expended in these efforts will be reported on in detail in the following sections.

II DISCUSSION

A. Circuit Techniques

1. Package Diode Performance

During the third quarter a packaged diode limiter was tested using diodes with a thin I-region for fast switching performance. These diodes were mounted in a low thermal resistance package which conforms to the CD-S8 outline and eliminates spring contacts, as seen in Figure 1. It was found that as much as 15 kilowatts peak power could be incident upon a pair of back-to-back placed diodes in shunt with the transmission line without diode burnout. This basic limiter circuit is shown in Figure 2. Actually the diodes were not tested to destruction due to arcing that occured in the tuning capacitor, C_T. With two of these limiters used in a balanced duplexer more than 30 kilowatts of peak power could be sustained. Pertinent details of this test are tabulated below in Table 1.

Table I

Peak Power	20 KW
Pulse Length	0.7 μsec
Average Power	10 watts
Average Isolation	15 db @ 1.5 KW
	18 db @ 15. KW
Switched Isolation (100 ma/diode)	20.6 db
Low Level Insertion Loss	1.3 db
Frequency	1350 Mc

Table I (continued)

Diode Parameters:

C(0)	(Zero biased capacity)	3.5 pf @ 1 Mc
τ_1	(Thermal time constant)	0.2 - 0.4 msec
σ	(Thermal resistance)	5°C/watt
VB	(Breakdown voltage)	450 Volts

It is seen that the maximum isolation obtainable with this configuration is 20.6 db as obtained when the diodes were externally biased at 100 millamps each. This suggests that the diode's equivalent resistance was 5 ohms under high incident RF power, because the series reactance is presumed to be zero with capacitive tuning. It seems more likely that the diode resistance was of the order of 1 ohm corresponding to a tuned isolation value of 34 db. This discrepancy may have been caused by inadequate tuning or by transmission of harmonics to which the series tuning capacitor would not have represented as low an impedance. The average isolation obtained when the diodes become self-biased by application of a high power RF pulse was 18 db at 15 kilowatts as seen from the table. This value of isolation which is less than the switch isolation performance includes the effect of energy transmitted through the device while the diodes are assuming this short circuit impedance through self-bias. This degradation of isolation from the applied bias balue is an indirect indication of the diode switching speed and the spike leakage, although these values have not yet been measured separately.

2. Integrated Diode Junction Circuit

During the last quarter circuitry for use with an integrated water cooled diode mount was completed. This is similar to that shown in Figure 1 of the second quarterly report, and it is expected that high power testing can be performed on it in the fourth quarter.

B. The Integrated Junction

In this quarter several attempts were made to mount the diode junctions on a thin plate with glass capsulation as were built and tested during the second quarter. However, good electrical contact was difficult to obtain at the top of the diode and metallic strips used for this purpose were bulky and had a tendency to break the glass. For this reason a special package was made which would incorporate the low thermal path to a heat sink desired in an integrated junction but yet provide convenient contact to the top of the diode. The first diodes thus made had higher thermal resistance than was expected, of the order of $10^{\circ}C$ per watt; and this was caused by problems in the package construction. The low thermal resistance packages will incorporate a soldered strap as the top contact for the die, enhancing the mechanical construction and this is shown in Figure 3.

This package has a suitably low inductance so that series tuning may not be necessary.

III CONCLUSIONS

During the third quarter a limiter using packaged diodes was built which provided 18 db of isolation with 1.3 db of insertion loss at an incident power level of 15 kilowatts at 1350 Mc. Two of these limiters used in a balanced limiter would then have a power capability of 30 kilowatts. Further tests are expected to show that even higher power levels can be sustained because this test was limited by a tuning capacitor in the test circuit. This improvement in power handling capability of a package diode resulted from new packaging technique incorporating welded construction which produced a diode with a thermal resistance of approximately 5°C per watt.

During this quarter also a circuit designed for the integrated junction limiter was completed and diodes suitable for test are expected to be available in the fourth quarter. Diode junctions which were fabricated in a special package to obtain the advantages of the integrated diode and yet provide the mechanical strength of the package were tried. These were found to be unsuitable because of package construction problems. New packages similar to thesebut with a soldered strap contact instead of a solid disc at the top of the die will be tried in the coming quarter.

LIST OF ILLUSTRATIONS

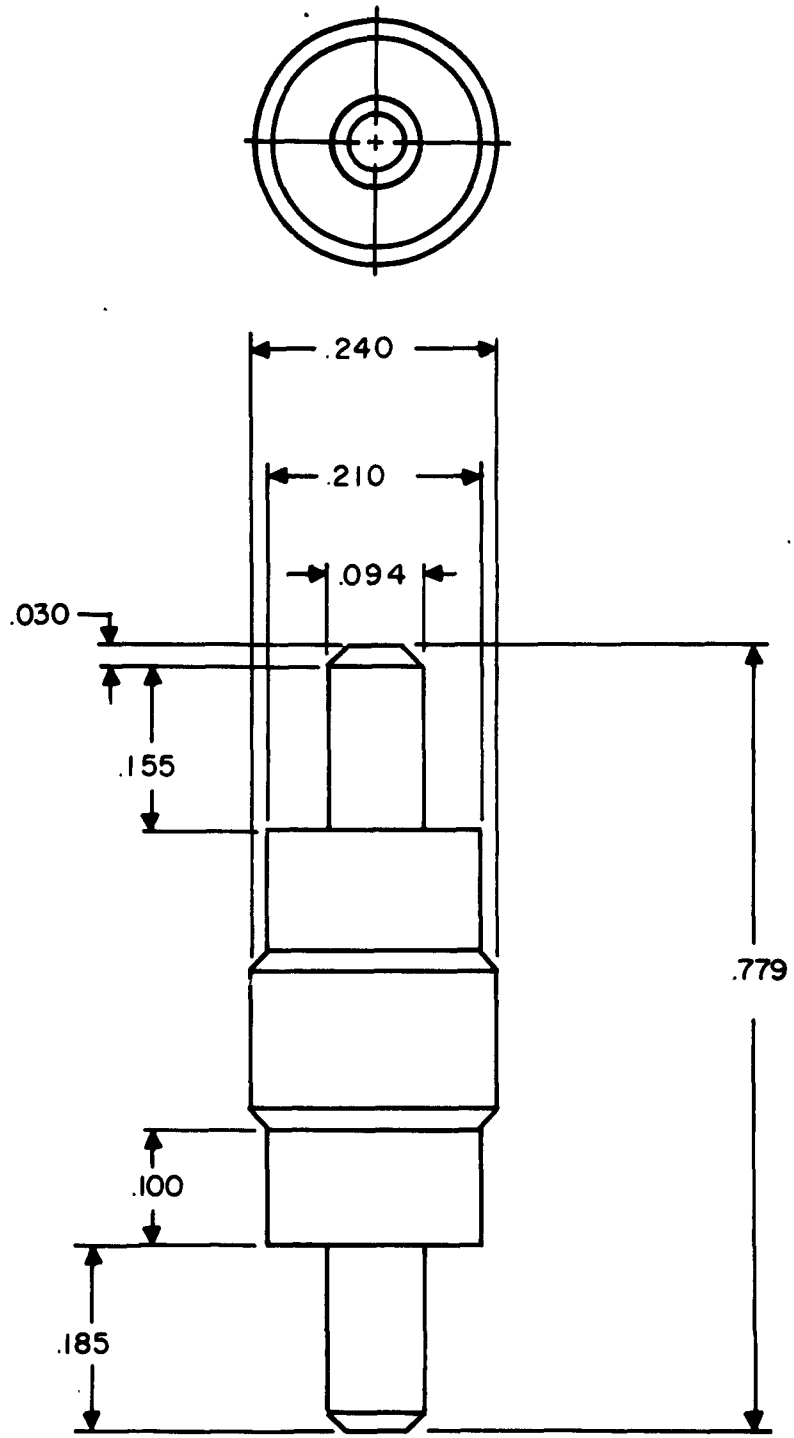
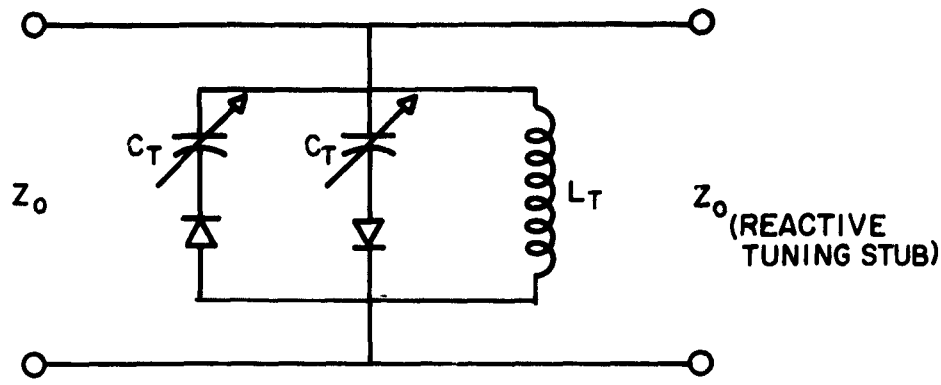
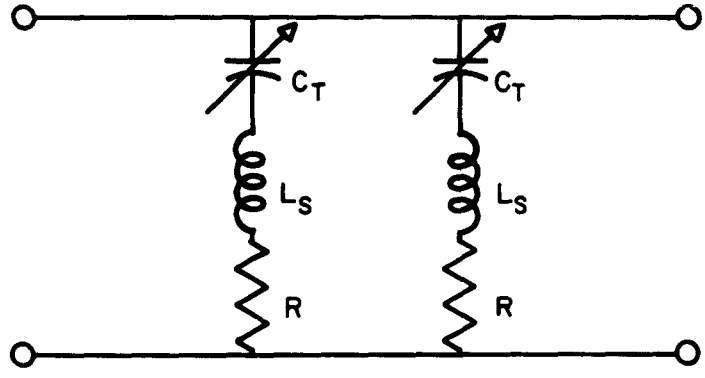


FIGURE 1

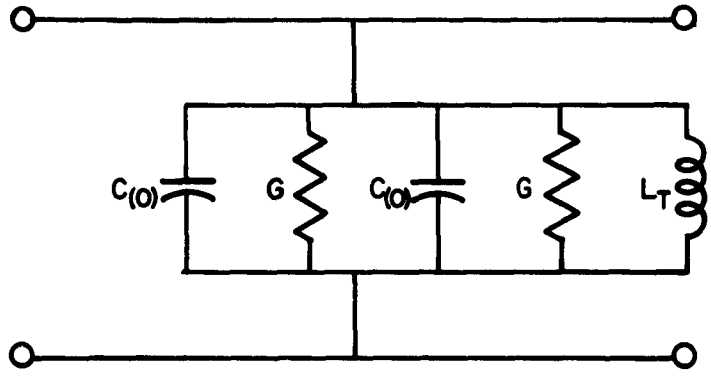
MICROWAVE ASSOCIATES PACKAGED DIODE OUTLINE OD-S-8



LIMITER CIRCUIT SCHEMATIC

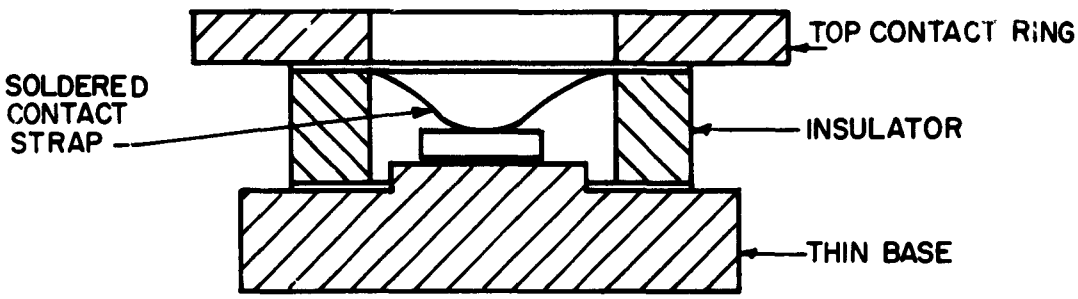


ASSUMED HIGH POWER EQUIVALENT CIRCUIT



ASSUMED LOW POWER EQUIVALENT CIRCUIT

FIGURE 2



LOW THERMAL RESISTANCE DIODE MOUNT

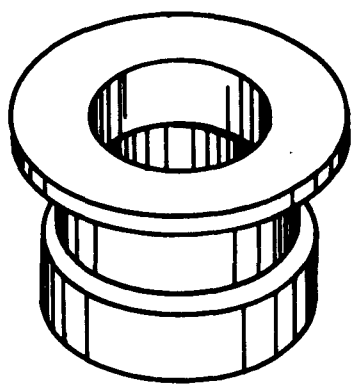


FIGURE 3

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